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# Reliability and failure analysis in power GaN-HEMTs during S-Band Pulsed-RF Operating

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## Abstract

This paper reports a reliability study on two technologies of AlGaIn/GaN high-electron mobility transistors (AlGaIn/GaN HEMTs) (Device "A" and Device "B"). A failure analysis study is conducted on devices stressed under real operating conditions for radar applications. The devices underwent pulsed-RF long ageing tests and after 11000h show a degradation in RF and DC performances (Drop of drain current and RF output power, pinch-off shift, decrease of the maximum of transconductance, lateral translation of transconductance, and increase of gate-lag and drain-lag). Hot electron effects are supposed to be the origin of the observed degradations and trapping phenomena within the passivation or GaN layers. Photon emission microscopy (PEM), Optical Beam Induced Resistance Change (OBIRCH), Electron Beam Induced Current (EBIC) measurements concur with this hypothesis. The three techniques reveal a non-uniform response and an inhomogeneous distribution along the gate fingers, in addition to the presence of some localized spots localized on the gate edge either on the drain side or on the source side. Spectral PEM analysis of these spots identifies a native defect that could be related to crystallographic defects such as dislocations or impurities. Atom probe tomography (APT) analysis on the two technologies of AlGaIn/GaN HEMTs supports this hypothesis. APT results show the presence of some chemical impurities like carbon and oxygen. These impurities are in relatively significant concentrations in device "A" which could explain the high level of gate-lag and drain-lag in this device compared to device "B".

**Key words:** Gallium Nitride High-electron mobility transistors (GaN HEMTs), RF-stress, Reliability, Failure analysis, Photon emission microscopy (PEM), Electron Beam Induced Current (EBIC), Optical Beam Induced Resistance Change (OBIRCH), Atom probe tomography (APT).

## 1. Introduction

AlGaIn/GaN high electron mobility transistors (HEMTs) outstanding electrical performances in high-power and high-frequency operating conditions [1, 2, 3] are considerably exceeding those of other semiconductor-based devices. This is due to the exceptional physical properties of Gallium Nitride (Wide band gap, high saturation electron velocity and high mobility) [4]. However, the use of these devices for power applications requires not only excellent performance but also long-term stability and high voltage capability.

To determine the lifetime of AlGaIn/GaN HEMTs and to investigate the reliability of this technology, long-term reliability tests, with a stress level close to the real operating conditions, have to be performed. For radar applications, pulsed-RF long duration ageing tests (11000 h) have been conducted on two power amplifiers (Supplier "A" devices and Supplier "B" devices) using AlGaIn/GaN HEMTs and described in [5]. The authors reported a drift of RF and DC performances of the aged transistors which is attributed to trapping phenomena. For in-depth reliability assessments and better understanding of the failure mechanism, this paper presents failure analysis study

on the aged devices of [5] using an experimental methodology based on different techniques: photon emission microscopy (PEM), Optical Beam Induced Resistance Change (OBIRCH), Electron Beam Induced Current (EBIC) and Atom probe tomography (APT). This methodology allows to compare reliability of two AlGaIn/GaN technologies.

## 2. Ageing test: Conditions & Main results

The devices studied in this work are two commercial AlGaIn/GaN HEMTs on SiC substrate from two different foundries: Supplier "A" and Supplier "B". Both transistors are in a ceramic package and designed for S-Band. Each transistor consists of 20-gate fingers of 250 $\mu$ m width and T shape gate. The device "A" has a voltage and current rating of 30 V and 5 A respectively, and the device "B" has a voltage and current rating of 43.5 V and 5 A respectively. The device "A" has a gate length of 0.25 $\mu$ m for a total development of 5.5mm. A field plate with a source termination is used in this transistor. The device "B" has a 0.5 $\mu$ m gate length (total gate development of 5 mm), 7.6 $\mu$ m source/drain spacing and 1.13 $\mu$ m source/gate spacing. Both devices have a 2nm GaN cap layer and are covered by SiN passivation layer.

The RF tests conducted on [5] are defined to be close to operational radar conditions as it is summarized in the Table

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1. The devices are stressed at 3-GHz operating frequency with a duty cycle (DC) equal to 80% and a compression around 6 dB for Supplier "A" devices and 4 dB for Supplier "B" devices. The DUTs have been run for 11000h at a quiescent current ( $I_{dq}$ ) corresponding to a class-AB amplification close to  $V_{ds(max)}$  ( $V_{DS0}=30V$  and  $I_{dq}=1.09mA/mm$  for "A" amplifiers and  $V_{DS0}=43.5V$  and  $I_{dq}=20mA/mm$  for "B" amplifiers). The junction temperature ( $T_j$ ) during the stress is estimated using pulsed IV measurements at different temperatures and dissipated powers [6].  $T_j$  is estimated at  $208^\circ C$  for Supplier "A" devices and  $210^\circ C$  for Supplier "B" devices.

Table 1: Ageing conditions of AlGaIn/GaN HEMTs

Foundry	Reference	Test Conditions
Test1	Supplier "A"	DutyCycle = 80%; 6dBc; f=3Ghz $V_{DS0}=30V$ ; $I_{dq}=1.09mA/mm$ $T_{baseplate} = 120^\circ C$ ; $T_j = 208^\circ C$
	A04_Ref	$T_{baseplate} = 120^\circ C$ ; $T_j = 120^\circ C$
Test2	Supplier "B"	DutyCycle = 80%; 4dBc; f=3Ghz $V_{DS0}=43.5V$ ; $I_{dq}=20mA/mm$ $T_{baseplate} = 130^\circ C$ ; $T_j = 210^\circ C$
	B04_Ref	$T_{baseplate} = 130^\circ C$ ; $T_j = 130^\circ C$

Following the ageing tests performed in [5], the authors noticed a drift of many electrical parameters as it is summarized in Table 2. First, they observed a small decrease in output power (-0.5 dB for "A" devices and -0.4 dB for "B" devices) and drain current (drift less than 14 % for "A" devices and lower than 7 % for "B" devices). The maximum of  $G_m$  ( $G_{mmax}$ ) decreased and a lateral translation of the transconductance curves has been noticed in addition to threshold voltage shifts. This suggests that the stress caused a variation in the quantity of traps located under the gate and between Gate-Source (G-S) or Drain-Source (D-S) at the AlGaIn/GaN interface [7, 8, 9]. An evaluation of drain-lag (DL) and gate-lag (GL) is supporting this hypothesis. The authors observed an increase of the drain-lag (around 10%) and the gate-lag (close to 2%) for the Test1 devices and a slight decrease of these parameters (around 2%) for the Test2 devices [5]. Moreover, the measurements show that supplier "A" devices present higher DL and GL levels than supplier "B" devices. Therefore supplier "A" devices are more sensible to trapping effects and could be more vulnerable to a failure in a radar application. According to literature, the decrease of output power and drain current is attributed to gate-lag effects that become more important after the stress [10, 11] and the drop of  $G_{mmax}$  is caused by hot electron effects [12, 13].

To give an accurate explanation on the degradation of DC and RF performances and to study possible physical degradations, failure analysis has to be performed.

Frontside opening was conducted and the ceramic cap of the transistors frame was removed to allow die investigation with photon emission microscopy (PEM), Optical Beam Induced Resistance Change (OBIRCH) and Electron Beam In-

duced Current (EBIC).

### 3. Failure analysis of Supplier "A" devices

#### 3.1. Device "A": PEM characterizations

PEM is a very efficient failure analysis tool usually used to study the reliability of semiconductor devices and to localize the degradations. This technique is used in many studies on AlGaIn/GaN HEMTs for different purposes. It helped reveal the presence of impact ionization in AlGaIn/GaN HEMTs [14], localize electronic traps produced in the devices during stress [15, 16], monitor the degradation of AlGaIn/GaN HEMT devices [17], analyze stress-induced percolation path [18], and evaluate the impact of the surface oxidation [19]. In this paper, PE analysis are conducted on fresh and stressed AlGaIn/GaN HEMTs in the on-state and the off-state operation modes. It has been noticed that all stressed devices present the same PE response.

PEM observations have been made using the HAMAMATSU microscope PHEMOS 1000. Images are acquired under the same DC bias conditions with the same exposition time (10s), detector sensitivity and colour scale.

Fig. 1 compares the PE signature of fresh reference device with the aged device "A02" in the on-state operation mode ( $V_{ds} = 30V$  and  $I_{ds} = 2.72mA/mm$ ) for two magnifications (x5) and (x20). It can be noticed that the fresh reference device "A05" shows an uniform PE distribution localized along all gate fingers. However the aged device presents an inhomogeneous light emission along each gate finger with higher intensity at the center of fingers. This is due to the non-uniformity of the temperature distribution which is higher in the center of the fingers, as observed from infrared microscopy measurements. Moreover, it can be observed that the electroluminescence at central fingers is more intense than the peripheral fingers. This is probably due to a shift of the pinch-off voltage that could be higher for the central fingers than the peripheral fingers. Indeed, the light intensity depends on both current flow and electric field, implying that the drain current distribution among fingers is probably irregular. Since the gate voltage  $V_{gs}$  is uniformly distributed, the pinch-off voltage may have shifted more negatively at the centre of the die rather than at the edge.

In the off-state operating mode ( $V_{ds} = 30V$  and  $V_{gs} = -7V$ ), the reference device ("A05") had low leakage current ( $8.36\mu A/mm$ ), and did not show any PE inhomogeneities. However, the aged devices presented a non-uniform luminescence along the gate fingers and very localized hot spots (Fig. 2-c). The PE response in this case is attributed to the increase of reverse gate leakage current. The hot spots observed may be due to the presence of native intrinsic crystal defects, with local changes in the electric field [20] or a current leakage path.

In order to localize more precisely the position of the emission, a higher magnification (x100) is used for PEM measurements. Fig. 2 presents the PE images of the fresh reference device "A05" and the aged devices "A01" and "A02". It can be noticed that the photon emission signature, in the on-state and off-state modes, is located at the edge of the gate on the

Table 2: A summary table of the ageing test results

	$I_{ds}$	$P_{out}$	$I_g$	PAE	$n, \Phi_0$	GL	DL	$R_{ds(on)}$	$V_{th}$	$G_{m(max)}$
Device "A"	↘ (< 14%)	↘ (0.5 dB)	↗	↘ ( $\approx 4\%$ )	Stable	↗ ( $\approx 2\%$ )	↗ ( $\approx 10\%$ )	↗	↘	↘
Device "B"	↘ (< 8%)	↘ (0.4 dB)	Stable	↘ ( $\approx 2\%$ )	Stable	↘ ( $\approx 2\%$ )	↘ ( $\approx 2\%$ )	↗	↗	↘

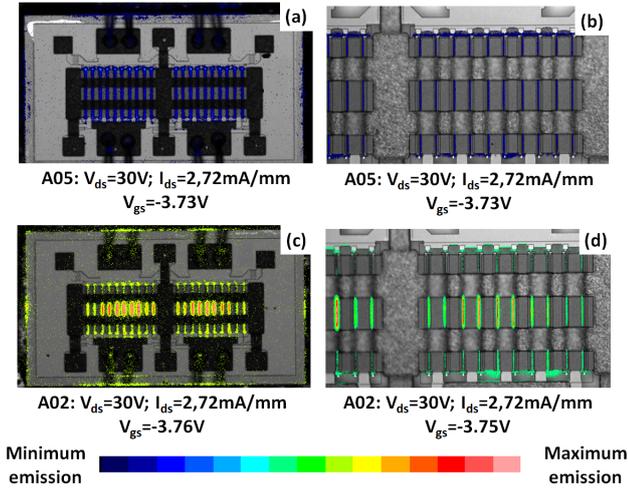


Figure 1: Comparison of front side PE images in on-state mode ( $V_{ds} = 30V$ ,  $I_{ds} = 2.72mA/mm$ ) with (x5) magnification (a-c) and (x20) magnification (b-d): (a-b) A05 reference device, (c-d) A02 aged

drain side. Two hot spots are observed in the off-state mode on the aged device "A01". Spectral photon emission microscopy (SPEM) is used to extract the fingerprint of these spots and to determine their origin.

### 3.2. Device "A": Spectral PEM

Using a diffraction grating placed in the optical path of the PE microscope [21], the PE spectrum of the defects can be extracted. Fig. 3-b presents the diffraction pattern image that shows the diffraction lines connecting the orders '0' and '1' from which the PE spectra are extracted (Fig. 3-c). It can be noticed from the PE spectra of the two spots of the aged device "A01", that the defects have the same cause. Indeed, the two distributions are centered on 836 nm which corresponds to an energy level of 1.48 eV. This trap has already been observed on a fresh device of the same technology [22] suggesting that it is probably a native defect. In [23], the authors found the same trap with DLTS on Schottky InAlN/GaN but its origin is still unknown. According to literature this type of defects may be attributed to intra-band transitions of highly energetic electrons, to intra-band transitions of electrons assisted by phonon, to direct transitions of electrons between bands, or to recombination via deep levels [24, 25, 23, 26, 27].

### 3.3. Device "A": OBIRCH vs EBIC

An OBIRCH analysis in Gate-Source diode mode at ( $V_{gs} = +1V$ ) with an orientation of frame of  $270^\circ$ , was carried out on

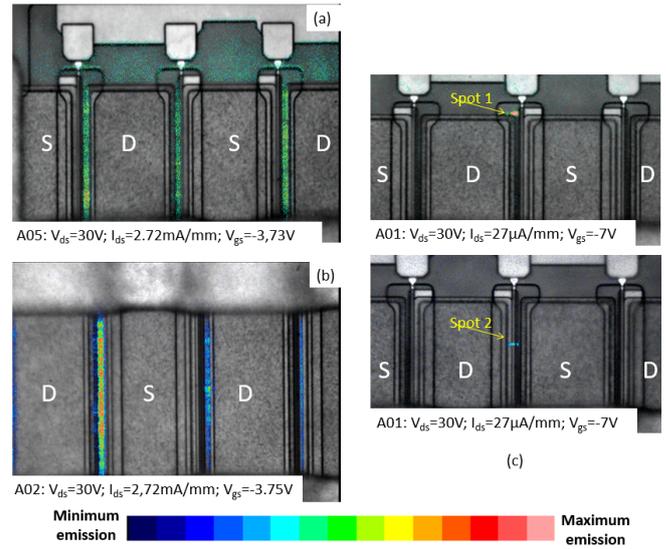


Figure 2: Localisation of the front side emission with (x100) magnification in on-state mode ( $V_{ds} = 30V$ ,  $I_{ds} = 2.72mA/mm$ ): (a) A05 reference device, (b) A02 aged, (c) Localisation of the A01 spots in off-state mode ( $V_{ds} = 30V$ ,  $V_{gs} = -7V$ )

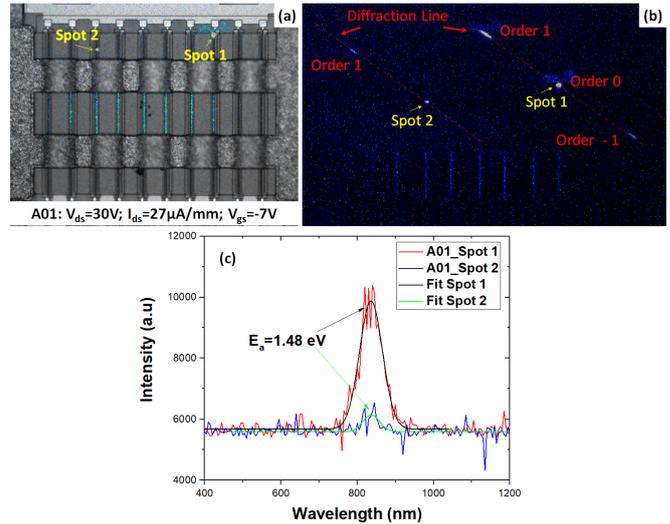


Figure 3: (a): A01 spot localisation (front side of the device); (b): Front side PE image of the diffracted spots; (c) Photon emission spectrum of "A01" spots

the reference device "A05" and the aged devices. All aged devices presented the same OBIRCH response. Fig. 4 compares the OBIRCH maps of The aged amplifier "A02" with the reference device. It is observed that the reference device does not

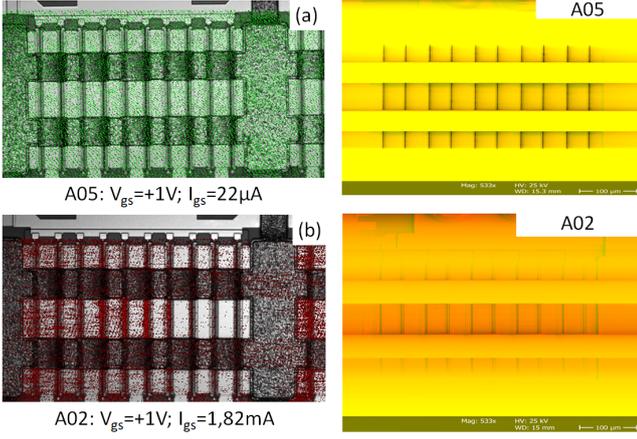


Figure 4: Left: OBIRCH images in Gate-Source diode Mode: (a): A05,(b): A02. Right: EBIC images: (a): A05,(b): A02

present any significant variation of the current unlike the aged device that shows a strong variation of current on:

- The peripheral fingers located on the left side of the chip
- The central fingers on the right side of the chip

No current variation was observed on the other fingers. This could suggest that there is a degradation of some fingers more than others on the aged devices.

EBIC measurements were carried out in a FEI PFIB Helios G4 CXe SEM system equipped with Nano-manipulators from Imina Technologies used to connect the device in the SEM chamber. The EBIC signal is collected between the drain and the source while the device is in the off-state operating mode ( $V_{gs} = -7V$ ). Measurements are performed on the reference device "A05" and the aged devices with an acceleration voltage of 25 keV and a current of 1.6nA. All aged devices presented the same EBIC response. Fig. 4 presents the EBIC measurements on the reference device "A05" and the aged device "A02". EBIC images show the presence of a strong induced current along the gate fingers of the reference transistor. On the aged device, it turns out that the distribution of the induced current is not uniform along the fingers, and that the current in the central fingers is more intense than in the peripheral fingers. These findings are matching the PEM and OBIRCH results.

#### 4. Failure analysis of Supplier "B" devices

##### 4.1. Device "B": PEM characterizations

The amount of photons emitted depends on the current density and the electric field in the structure. Failure analysis were carried out on two fresh "B" type devices ("B05" and "B06") in order to visualize the effect of fields and current on the intensity of photoemission. The Fig. 5 presents the PE images of the reference devices polarized in on-state mode. Fig. 5-a and b show the PE maps at two different voltages ( $V_{DS} = 30.5V$  and  $V_{DS} = 43.5V$ ), and Fig. 5-c and d show the PE maps at two different

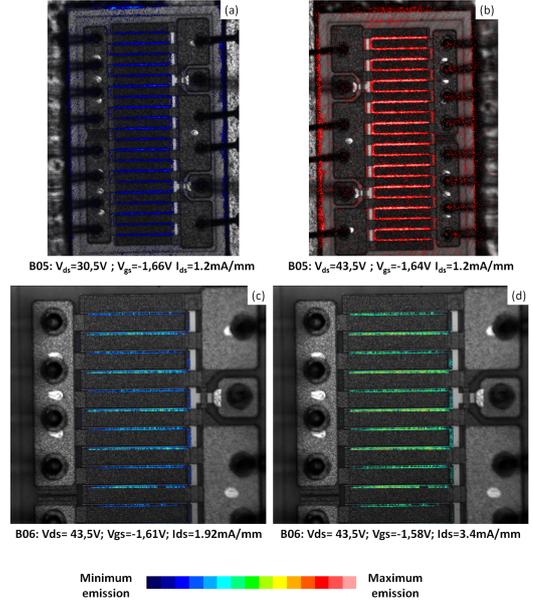


Figure 5: Comparison of front side PE images of a fresh reference device "B05" in on-state mode ( $I_{ds} = 1.2mA/mm$ ): (a) at  $V_{DS} = 30.5V$ , (b)  $V_{DS} = 43.5V$

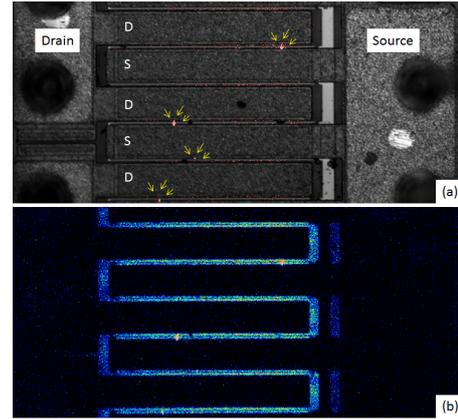


Figure 6: "B05" front side PE image with (x20) magnification: (a) Zoom on the high intensity spots, (b) Zoom on the gate fingers.

current densities ( $I_{ds} = 1.92mA/mm$  and  $I_{ds} = 3.4mA/mm$ ). It can be noticed that the higher the drain-source field or/and the current density, the higher the intensity of the photon emission. It can be noticed also that the PE distribution of the fresh reference devices is not completely uniform on the surface of the devices. Some fingers are brighter than others and the emissions are not homogeneous along the gate fingers which can be attributed to the non-uniformity of the temperature distribution. Moreover, we observed various high intensity spots are noticed (yellow arrow) located under the gate on the source side (Fig. 6).

The aged "B" type devices of Test 2 ("B02" and "B03") are analyzed with the front side PEM technique. Fig. 7 presents the comparison of the PE signature of the fresh reference device "B06" with the aged devices in the on-state mode at  $V_{ds} = 43.5V$  and  $I_{ds} = 1.92mA/mm$ . It can be observed that the PE

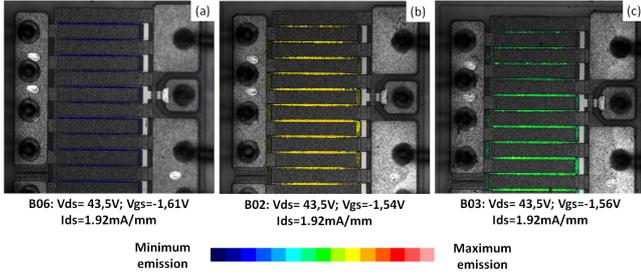


Figure 7: Comparison of the front side PE signature of the fresh reference device "B06" with the aged devices in the on-state mode at  $V_{ds} = 43.5V$  and for two current densities:  $I_{ds} = 1.92mA/mm$  and  $I_{ds} = 3.4mA/mm$ . (a-b): "B06", (c-d): "B02", (e-f): "B03".

intensity is higher for the aged devices, in particular for the device "B02". It is also noted that the "hot spots" are more present on the aged devices than on the reference device "B06". This probably reveals the location of the leakage paths.

#### 4.2. Device "B": OBIRCH vs EBIC

An OBIRCH analysis in off-state mode at ( $V_{ds} = 25V$ ,  $V_{gs} = -7V$ ,  $I_{ds} = 1.15\mu A/mm$ ) with an orientation of frame of  $270^\circ$ , was performed on the reference device "B05".

When the component is strongly pinched off, an increase in the current variation is observed on the fingers of the transistor. The distribution of the OBIRCH signal is non-uniform and occurs as forming spots along the fingers. OBIRCH response on device fingers is poor. There is a great resemblance between the OBIRCH mapping and the PE mapping of the component under test when it is biased in strongly pinched off transistor mode (Fig. 8-a and 8-b).

EBIC measurements are carried out at an acceleration voltage of 25 keV and a current of 1.6nA. The signal is collected between the drain and the source while the device is in the off-state operating mode ( $V_{gs} = -7V$ ). The EBIC images on a fresh reference device "B05" (Fig. 8-c) identify the presence of a strong current induced along the gates of the transistor. It is noted that the distribution of the induced current is not uniform along the fingers, and more intense spots are observed. These spots can indicate leakage paths which may be related to electrically active defects like dislocations or impurities in the crystal lattice [28]. To check this hypothesis a physical failure analysis on the atomic-scale must be conducted. Atom probe tomography is used next on the two devices "A" and "B" to identify the differences between those two components and to help explain the electrical and the PE results.

### 5. Atom Probe tomography

Atom probe tomography (APT) is a recent technique in the field of microelectronics and has the capacity to analyse materials and devices chemically in 3D at almost atomic scale [29]. This technique has e.g. recently shown the capacity of detecting magnesium segregation to threading dislocation in GaN HEMT device [30]. Devices A and B were analysed by APT. Prior

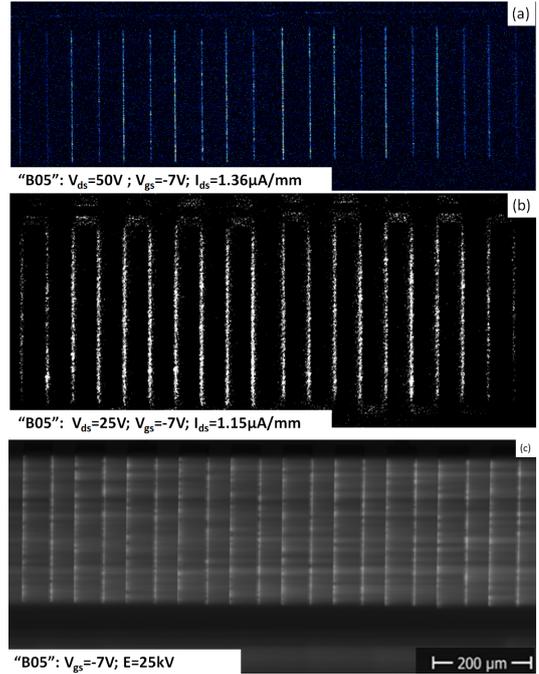


Figure 8: Comparison of the response of the reference device "B05": (a) Back side PEM image in off-state mode, (b) OBIRCH image in pinch-off mode ( $V_{ds} = 25V$ ,  $V_{gs} = -7V$ ,  $I_{ds} = 1.15\mu A/mm$ ), (c) EBIC image

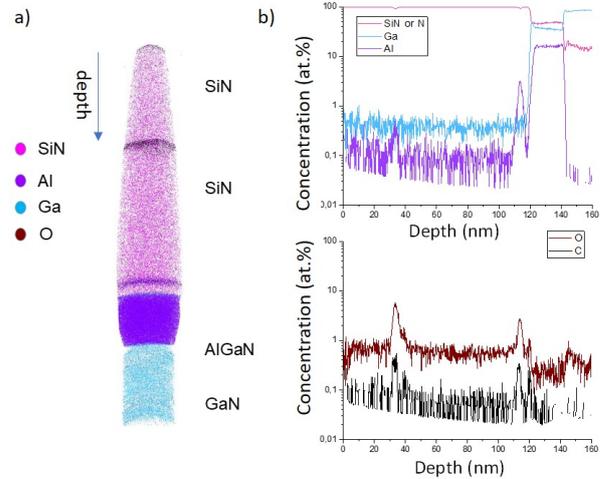


Figure 9: APT analysis of component A. a) image of the 3D reconstruction of dielectric/semiconductor interface (each dot represents one atom) and b) Concentration profiles of elements as a function of depth

to the analysis, the sample has to be shaped as a nanotip using Focused-Ion-Beam (FIB) technique. More details concerning APT analysis and SEM/FIB preparation procedure can be found in [30] and APT data treatment procedures can be found in e.g. the following reference [31]. The location of analysis for both samples was chosen at the dielectric (SiN)/semiconductor (GaN/AlGaIn/GaN) interface, close to the gate region. Figure 9 and 10 shows the APT analyses of the devices "A" and "B" fresh devices respectively. The shape of the 3D reconstruction depends mainly on the sample preparation. While the struc-

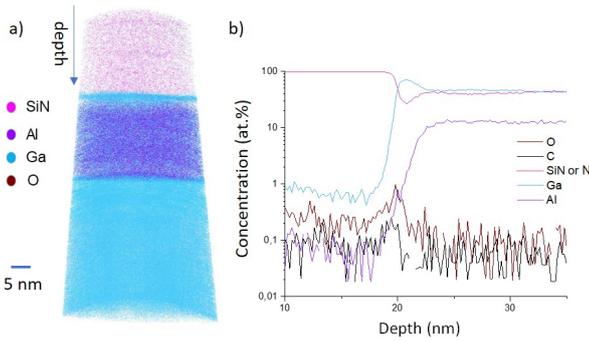


Figure 10: APT analysis of component B. a) image of the 3D reconstruction of dielectric/semiconductor interface (each dot represents one atom) and b) Concentration profiles of elements as a function of depth

ture of both components (dielectric/semiconductor stacking) is close for both structures (Fig 9-a and 10-a), the main differences are revealed by the depth profiling concentration analysis. Device "B" shows indeed less chemical impurities like carbon and oxygen. The latter are found in the dielectric layer of device "A" what was not observed in device "B". The concentration profile also evidenced a slightly higher C and O at the dielectric/semiconductor interface in device "A". This could explain the high level of gate-lag and drain-lag in device "A" comparing to device "B". Indeed, the impurities may act as border traps or/and interface traps which quantity may vary with the stress leading to a degradation of the electrical parameters specially GL and DL. In order to confirm this hypothesis, physical simulation must be conducted [9, 32]. APT measurements of the device "A" revealed also the presence of an Aluminium-rich layer in the dielectric, few nm above the semiconductor (Figure 9). The latter was also confirmed by a scanning transmission electron microscopy technique. Several analyses were performed to confirm the results. The quality of the process is then thought to be part of the electrical characteristics differences observed between components and might play a role during ageing, thus affecting their reliability.

## 6. Conclusion

This paper presents a failure analysis study of two technologies of AlGaIn/GaN HEMTs using various techniques: PEM, OBIRCH, EBIC and APT. The studied devices underwent pulsed-RF long duration ageing tests. The tests induce variations in the DC and RF performances which are most significant for supplier "A" devices (Drain current and RF output power drop, shift of threshold voltage, decrease in the maximum transconductance peak, increase of gate-lag and drain-lag). These degradations are related to hot electron effects and traps located on the bulk under the gate or between G-S or G-D. This hypothesis is confirmed by photoemission measurements that show a strongly inhomogeneous distribution and the presence of some hot spots. The spots are located at the edge of the gate on the drain side for supplier "A" devices, and they are located under the gate on the source side for supplier "B" devices. PE measurements conducted on supplier "B" devices at different values

of  $V_{ds}$  and current density show that the higher the electric field or the current density, the higher the intensity of PE. A great resemblance was noticed between the PE mapping in the off-state mode, the OBIRCH mapping and the EBIC mapping of the supplier "B" device. Indeed, the three techniques revealed a non-uniform distribution along the fingers, and the appearance of localized intense spots.

Spectrally resolved photoemission measurements in off-state operation mode, conducted on aged supplier "A" devices, identified a trap located at 1.48eV that has been already observed in fresh samples. This suggests that this trap is a native defect that could be related to crystallographic defects such as dislocations or impurities. Atom probe tomography measurements conducted on both devices "A" and "B" support this hypothesis. They reveal the presence of some chemical impurities like carbon and oxygen with higher amount on the device "A". These impurities and an eventual variation of their quantities with the stress may be the cause of the degradations observed on the electrical parameters specially the variations of drain-lag and gate-lag. In order to confirm this hypothesis, physical simulation must be conducted.

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